device comprising:

a gate region, the gate region including a gate and gate oxide;

a body region under the gate region;

an enhanced drift region under the gate region whereby the enhanced drift region purposely overlaps the body region; ~~and~~

a drain region within the enhanced drift region such that the enhanced drift region is under the entire drain region; and

a layer, well or substrate under the enhanced drift region and the body region, wherein the layer, well or substrate has the same conductivity type as the enhanced drift region.

6. (cancelled)

7. (original) The LDMOS device of claim 5 wherein the enhanced drift region purposely overlaps the lateral tail of the body region.

8. (withdrawn) A method for providing a lower Ron* product LDMOS device comprising the steps of:

(a) providing a gate region on a substrate;

(b) providing a body region on the substrate underneath the gate region; and

(c) providing an enhanced drift region under the gate region wherein an enhanced drift region purposely overlaps the body region.

9. (withdrawn) The method of claim 8 wherein the gate region is of such a length that the enhanced drift purposely overlaps the body region when the enhanced drift region is implanted in the substrate.

10. (withdrawn) The method of claim 8 wherein the body region is provided by implanting Boron ions into the substrate.

11. (withdrawn) The method of claim 10 wherein the enhanced drift region is provided by implanting phosphorous ions that are self-aligned with the gate region into the substrate.

12. (withdrawn) The method of claim 10 which further includes the step of (d) providing a field oxide region.

13. (withdrawn) The method of claim 12 wherein the enhanced drift region is not self-aligned with the gate region.

14. (withdrawn) The method of claim 12 wherein the enhanced drift region is provided before the field oxide region is provided.

15. (new) The LDMOS device of claim 1 wherein the enhanced drift region purposely overlaps the lateral tail of the body region.

16. (new). The LDMOS device of claim 1 wherein the conductivity type of the enhanced drift region and the layer, well, or substrate is N-type.

17. (new). The LDMOS device of claim 1 wherein the conductivity type of the enhanced drift region and the layer, well, or substrate is P-type.

18. (new). The LDMOS device of claim 1 wherein the layer, well, or substrate is an epitaxial layer, and further comprising a buried layer provided under the epitaxial layer and above a substrate, the buried layer having the conductivity type of the epitaxial layer and a different conductivity type than the substrate.

19. (new). The LDMOS device of claim 5 wherein the conductivity type of the enhanced drift region and the layer, well, or substrate is N-type.

20. (new). The LDMOS device of claim 5 wherein the conductivity type of the enhanced drift region and the layer, well, or substrate is P-type.

21. (new). The LDMOS device of claim 5 wherein the layer, well, or substrate is an epitaxial layer, and further comprising a buried layer provided under the epitaxial layer and above a substrate, the buried layer having the conductivity type of the epitaxial layer and a different conductivity type than the substrate.